WHAT IS CLAIMED IS:

1. A method for transferring multiple bits of data across asynchronous clock domains comprising the steps of:

detecting a change in a status bit of a data word being transferred from a source in a source clock domain to a destination register in a destination clock domain, the source clock and destination clock being asynchronous;

sampling the detected change in reference to a change window, the change window sized to encompass all bits of the data word;

selecting a stable input for each bistable circuit of the destination register based on whether the detected change in the status bit is likely to produce metastability in the receiving register.

2. The method of claim 1, further comprising:

registering the data and a status bit in a source register clocked by the source clock.

3. The method of claim 1, further comprising:

toggling the status bit for each word of data to be transferred to the destination clock domain.

4. The method of claim 1, further comprising:

connecting each output of the source to an input of a receive register which is comprised of a group of multiplexers each coupled to an input of a corresponding bistable circuit, each multiplexer configured to receive a signal selecting the stable input.

5. The method of claim 1, further comprising:

outputting a control signal to select the stable input for each bistable circuit of the receive register if transitions in the change window are likely to induce metastability in the receive register.

6. The method of claim 5, further comprising:

selecting one of two inputs in response to the monitoring circuit control signal for storage in the flip-flop.

7. The method of claim 1, further comprising:

clocking the receive register flip-flops with a delayed copy of the destination clock.

8. The method of claim 1, wherein the bistable circuits include one of flip flops and latches.

9. The method of claim 1, wherein the source includes a FIFO.

10. The method of claim 1, wherein the source includes a RAM.

11. The method of claim 1, further comprising transferring a data word from the source to a plurality of destination registers.

12. A circuit for transferring multiple bits of data across asynchronous clock domains comprising:

a source clocked by a first source clock, the source storing a data word and a status bit; and

a receiving circuit including:

a monitoring circuit, wherein one input is operatively coupled to receive a status bit output of the source, a second input operatively coupled to receive a destination clock, and an output operatively coupled to control inputs of a group of multiplexers;

a delay element having an input operatively coupled to the destination clock and an output operatively coupled to a clock input of a destination register;

a first group of delay elements including a plurality of delay elements equal in number to a number of bits in the source, wherein each delay element of the first group of delay elements has an input operatively coupled to one source output;

a second group of delay elements including a like plurality of delay elements, wherein each delay element of the second group of delay elements has an input operatively coupled to a same source output as a corresponding delay element in the first group of delay elements;

a destination register having data inputs operatively coupled to the outputs of the group of multiplexers, the group of multiplexers being equal in number to a number of bits in the destination register, wherein each multiplexer has a first data input operatively

coupled to receive a signal from an output of a corresponding delay element of the first group of delay elements and a second data input operatively coupled to receive a signal from an output of a corresponding delay element of the second group of delay elements.

13. The circuit of claim 12, further comprising a plurality of receive circuits.

14. The circuit of claim 12, wherein the source includes a register.

15. The circuit of claim 12, wherein the source includes a FIFO.

16. The circuit of claim 12, wherein the source includes a RAM.

17. The circuit of claim 12, wherein the destination register includes flip-flops.

18. The circuit of claim 12, wherein the destination register includes latches.

19. The circuit of claim 12, wherein the second data input of each multiplexer of the group of multiplexers is operatively coupled to a static signal.

20. The circuit of claim 12, wherein the second data input of each multiplexer of the group of multiplexers is operatively coupled to an output of the destination register.